12.1 A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/Conversion-Step

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Low-power ADCs are key elements in display and imaging systems. For the ADCs of such systems, the required ENOB exceeds 9 while the sampling rate (f_s) and ERBW requirements are proportional to the number of pixels and the refresh rate of the display system. At the same time the power consumption of the ADCs should be low especially for (portable) systems incorporating more than one ADC. If the ADC is not always running at a fixed (maximum) f_s, then speed-on-demand, i.e., the ability to program the sampling rate to maintain a good power/speed ratio, is essential for a power efficient design. A well-known FOM that relates power consumption to speed and accuracy of the ADC is given by Equation 1.

$$\text{FOM} = \text{Power} / (2^{\text{ENOB}} \times f_{s,nyq}) \quad (1)$$

A FOM of 1pJ has been reported for 10b ADCs optimized at one f_s [1][2][3][4] while ADCs with programmable speed and power show a FOM of 1.5pJ [5]. In this paper, an ADC with programmable speed and power is presented that achieves a FOM of 0.5pJ over a large range of sample frequencies. The ADC is fabricated in a 90nm digital CMOS process. The chip operates from a 1.2V supply and occupies 0.3mm^2.

In high-speed low-power ADCs the use low supply voltage for the fast submicron CMOS transistors implies a reduced signal swing. Therefore, maintaining a good SNR becomes a challenge. In this paper, an ADC topology is chosen that can operate from a 1.2V supply and is optimized for noise.

Figure 12.1.1 shows the block diagram of the pipelined chain. For low noise, it is important that the first stage in a pipelined ADC combines high frequency input sampling and signal amplification. In this way, only one opamp contributes to the noise. The first gain stage is a 2.5b stage consisting of a single opamp and six comparators. It performs sampling of the high-frequency input signal and four times residue signal amplification. The following 7 gain stages are 1.5b stages consisting of a single opamp and two comparators. They perform sampling of the S/H signal of the previous stage and two times residue signal amplification. Because the first stage has a signal gain of 4, the following 7 stages are scaled down for low power and area. The last stage is a 2b flash stage consisting of 5 comparators. This stage also provides the over-range detection. The output of all the comparators is fed to a digital encoder that produces the final output bits.

Each stage has a sample clock phase and a gain clock phase. During the sample clock phase the input is sampled on the sample capacitor C_s while the comparators compare the input signal with reference voltages. Depending on the output of the comparators, a reference voltage is subtracted from the sampled value and the residue signal is amplified by the opamp during the gain clock phase.

During both clock phases, noise is added to the signal. Figure 12.1.2 shows two sampling schemes. The first one is sampling to virtual ground. In this way, high-frequency opamp noise is added to the signal during sampling clock phase which will deteriorate the SNR. The advantage of this scheme is that the effects of the opamp offset and 1/f-noise are minimized. In this work, the second sampling scheme is chosen showing sampling to ground. In this case, only the switch noise is added to the signal during sampling clock phase. Furthermore, no bandwidth limitation is imposed on the opamp during the sampling of the input signal, resulting in a high ERBW independent of biasing. The opamp offset and 1/f-noise are kept low by choosing large input transistors for the opamp.

The opamp DC-gain (A_0) and unity-gain bandwidth (f_t) are derived for accurate and fast settling during the gain clock phase. To program the speed and power of this ADC, a constant A_0 over a large range of bias currents is required while f_t should scale with the bias current. These requirements can be met using a differential two-stage Miller opamp, where the first stage consists of a folded cascode amplifier (see Fig. 12.1.3). For this topology, A_0 is proportional to the ratio of the transconductance (g_m) and the output conductance (g_o) of the MOS transistors. Therefore, an A_0>65dB is achieved over a large bias range. The opamp's f_t is determined by the ratio of its g_m and the Miller capacitor C_{Miller} where g_m scales with the bias current.

For good phase margin at high frequencies, a resistor is added in series with the Miller capacitor. Usually, this resistor is the reciprocal of the transconductance of the output transistor. This transconductance is dependent on the programmable bias current and consequesntly the resistor should also track the bias current. Hence, the resistor is implemented with a source follower N_M, as shown in Fig. 12.1.3, resulting in an optimal settling behaviour for all bias settings.

The circuit uses a supply voltage of 1.2V. Therefore, the value of the signal swing is chosen to be $0.8V_{pp,diff}$ and transistors are carefully dimensioned in order to properly operate from the low supply voltage. The common-mode level of the differential output is determined by a switched-capacitor control loop (not shown in Fig. 12.1.3) and is set to slightly more than half the supply voltage.

Figure 12.1.4 shows the complete layout of the ADC. Capacitors are realized with standard backend M1-M5 plate structures. Power routing is done with wide M6 tracks on top of the gain stages to minimize series resistance and area. The total chip area is 0.3mm^2 including the digital encoder and the reference block.

Figure 12.1.5 shows the measured dynamic performance of the ADC. The curves in the upper plot show the ADC's ENOB as a function of f_s for several discrete power settings while operating from a 1.2V supply with f_{in}=10MHz. The curves in the lower plot show the ADC's ENOB, SNR, and THD as a function of f_{in} for a particular power and speed setting. Because of the sampling to ground technique, ERBW exceeds 100MHz. Figure 12.1.6 shows the plot of FOM, as defined in Equation 1, of this converter as well as a few previously published ADCs. With a FOM of 0.5pJ/conversion-step for a large range of sample frequencies, this figure shows the power efficiency of the proposed ADC. Figure 12.1.7 summarizes the ADC performance.

References:

[1] M. Yoshioka, et al., "A 10b 125MS/s 40mW Pipelined ADC in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 282-283, Feb., 2005.

[2] O. Stroeble, V. Dias, C. Schwoerer, "An 80MHz 10b Pipeline ADC with Dynamic Range Doubling and Dynamic Reference Selection," *ISSCC Dig. Tech. Papers*, pp. 462-463, Feb., 2004.

[3] B. Min, et al., "A 69-mW 10-bit 80-MSample/s Pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2031-2039, Dec., 2003.

[4] D. Miyazaki, S. Kawahito, M. Furuta, "A 10-b 30-MS/s Low-Power Pipelined CMOS A/D Converter Using a Pseudodifferential Architecture," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 369-373, Feb., 2003.

[5] B. Hernes, et al., "A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13µm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 256-257, Feb., 2004.

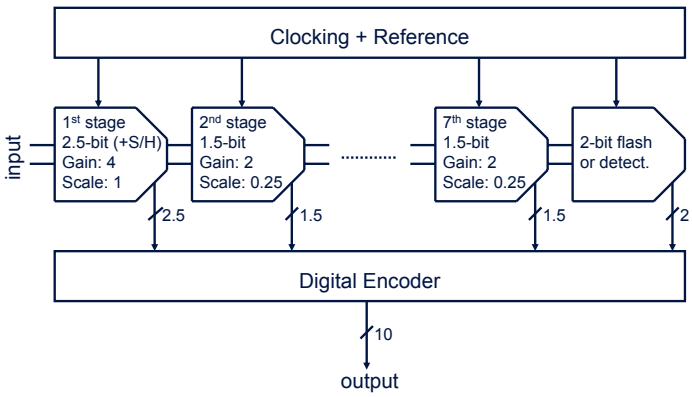


Figure 12.1.1: Block diagram of the proposed pipelined ADC.

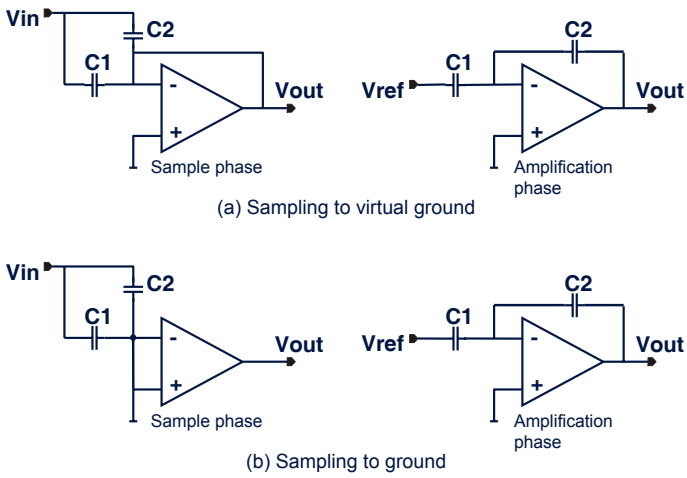


Figure 12.1.2: Sampling schemes.

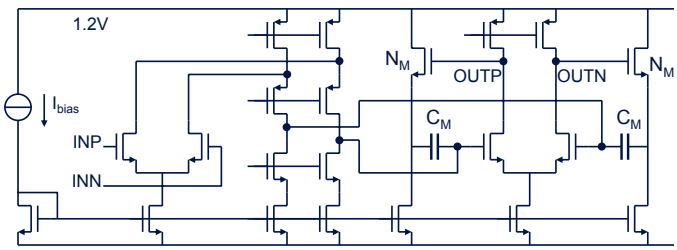
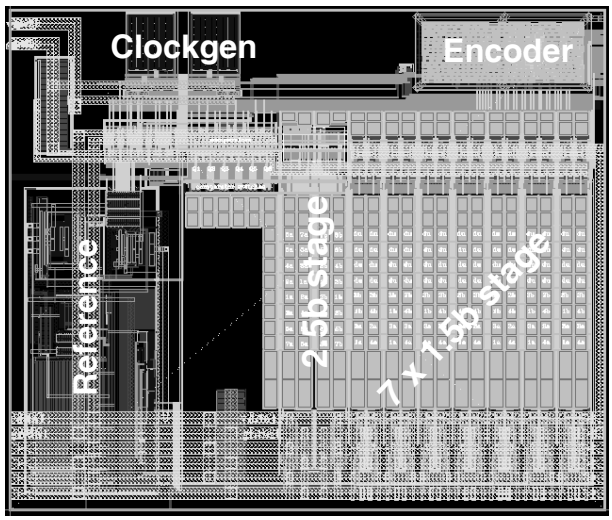


Figure 12.1.3: Schematic of the two-stage Miller opamp with variable I_{bias}.



600µm x 500µm = 0.3mm²

Figure 12.1.4: The complete layout of the ADC.

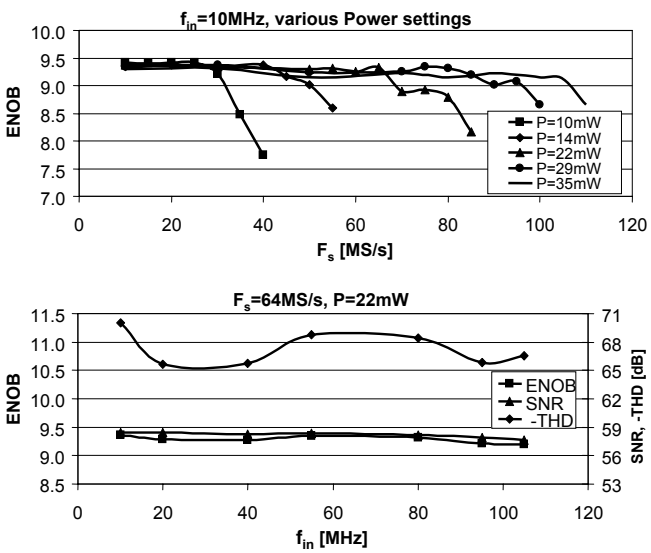


Figure 12.1.5: Measured dynamic performance.

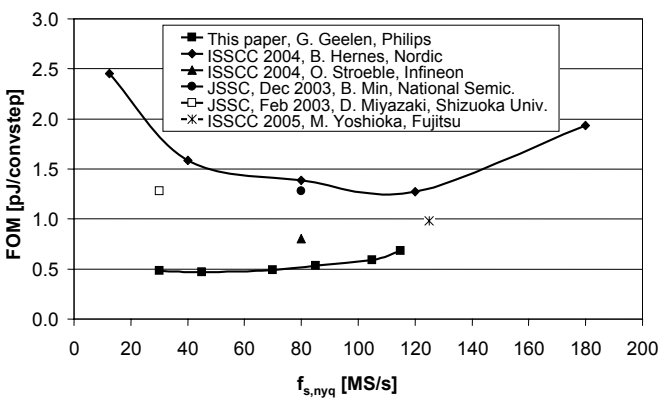


Figure 12.1.6: Measured FOM compared to previously published ADCs.

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Architecture	Pipeline 1x2.5b, 7x1.5b stages
Technology	90nm digital CMOS, 1poly, 6metal
Supply voltage	1.2V
Input range	$0.8V_{pp,diff}$
Resolution	10b
DNL/INL	< 1.0LSB
ENOB	9.3b
SNR	58.5dB
THD	< -65dB
ERBW	> 100MHz
Fs,max	25 - 120MSample/s
Cin	1.0pF
Area	$0.3mm^2$
Power	0.3mW/MSample
FOM	0.5pJ/convstep

Figure 12.1.7: Summary of the ADC performance.

